DS21354DK
T1 Single-Chip Transceiver Design Kit Daughter Card

www.maxim-ic.com

GENERAL DESCRIPTION

The DS21354 design kit is an evaluation board for the DS21354. The DS21354DK is intended to be used as a daughter card with either the DK2000 or the DK101 motherboards. The board is complete with a single-chip transceiver (SCT), transformers, termination resistors, configuration switches, line protection circuitry, network connectors, and an interface to the motherboard.

ORDERING INFORMATION

PART	DESCRIPTION
DS21354DK	DS21354 Design Kit Daughter Card

FEATURES

- Expedites New Designs by Eliminating First-Pass Prototyping
- Interfaces Directly to the DK101 or DK2000 Motherboards
- Demonstrates Key Functions of the DS21354
- High-Level Software Provides Visual Access to Registers
- Software Controlled (Register Mapped) Configuration Switches to Facilitate Clock and Signal Routing
- BNC Connections for 75Ω E1
- Bantam and RJ48 Connectors for 120Ω T1
- Multitap Transformer to Facilitate True Impedance Matching for 75Ω and 100Ω/120Ω Paths
- Network Interface Protection for Overvoltage and Overcurrent Events
- Testpoints and Prototype Area Available for Further Customization

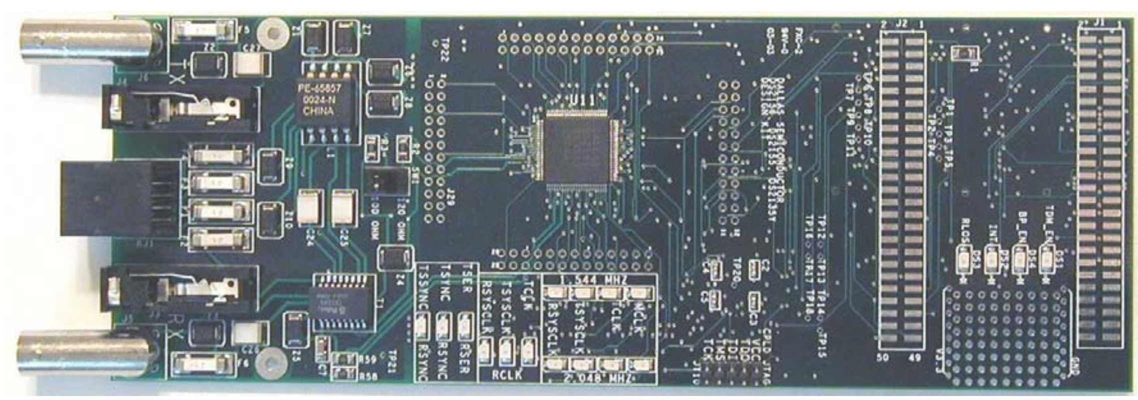


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COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C1–C5, C8–C12, C15–C19, C21, C22, C29–C34	23	0.1µF 10%, 16V ceramic capacitors (0603)	Digi-Key	311-1088-1-ND
C7, C36	2	1µF 10%, 16V ceramic capacitors (1206)	Digi-Key	PCC1882CT-ND
C13, C14	2	0.1µF 10%, 16V ceramic capacitors (0805)	Digi-Key	311-1142-1-ND
C23	1	0.1µF 10%, 25V ceramic capacitor (1206)	Digi-Key	PCC1883CT-ND
C24–C27	4	0.22µF, 50V ceramic capacitors	Digi-Key	UNK
C35	1	10µF 20%, 16V tantalum capacitor (B case)	Digi-Key	PCS3106CT-ND
DS1, DS4–DS18	16	LED, green, SMD	Digi-Key	P501CT-ND
DS2, DS3	2	LED, red, SMD	Digi-Key	P500CT-ND
F1–F6	6	250V, 1.25A fuse, SMT	Teccor Electronics	F1250T
J1, J2	2	Male 0.1, SMD, 50-pin, dual-row vertical	Samtec	TSM-125-01-T-DV
J3, J4	2	Bantam connectors	SWK	RTT34B02
J5, J6	2	Connector BNC RA 5-pin	Kruvand	UCBJR220
J7–J9	3	Socket, SMD, 50-pin, dual-row vertical	Samtec	TFM-125-02-S-D-LC
JT10	1	Connector, 10-pin, dual-row vertical	Digi-Key	S2012-05-ND
L1	1	Choke, dual 4-line 24µH, 8-pin SO	Pulse Engineering	PE-65857
R1, R14, R21	3	51.1Ω 1%, 1/8W resistors (1206)	Digi-Key	P51.1FCT-ND
R2, R3, R58, R59	4	0Ω 5%, 1/8W resistors (1206)	Digi-Key	P0.0ETR-ND
R4, R5, R60	3	51.1Ω 1%, 1/10W resistors (0805)	Digi-Key	P51.1CCT-ND
R6, R9, R10, R13, R15–R19, R22, R23, R25–R29, R32, R37, R38, R44, R47–R49, R61	24	10kΩ 1%, 1/10W resistors (0805)	Digi-Key	P10.0KCCT-ND
R7, R8, R11, R12, R30, R31, R35, R36, R39–R43, R45, R50–R53	18	330Ω 0.1%, 1/10W MF resistors (0805)	Digi-Key	P330ZCT-ND
R24	1	1.0kΩ 1%, 1/10W resistor (0805)	Digi-Key	P1.00KCCT-ND
R33, R34	2	NOPOP	—	NOPOP
R46	1	4.7kΩ 1%, 1/8W resistor (0805)	Digi-Key	9C08052A4701FKHFT
R54, R55	2	61.9Ω 1%, 1/8W resistors (1206)	Digi-Key	P61.9FCT-ND
R56, R57	2	49.9Ω 1%, 1/8W resistors (1206)	Digi-Key	P49.9FCT-ND
RJ1	1	RJ48 connector	Molex	43223
SW1	1	Switch DPDT slide 6-pin TH	Avnet	SSA22
T1	1	XFMR 16-pin SMT	Pulse Engineering	TX1099
U1–U4, U6	5	BBUS switch 10-bit CMOS, 150-mil, 24-pin SO	IDT	IDTQS3R861Q
U5	1	144-pin macrocell CPLD	Avnet	XC95144XL-10TQ100C
U7–U10	4	Quad bus switch, 150-mil, 16-pin SO	IDT	IDTQS3125Q
U11	1	T1/E1/J1 XCVR 100-pin QFP, 0°C to +70°C	Dallas Semiconductor	DS2156L
Z1, Z6–Z8	4	160V, 500A Sidactor	Teccor Electronics	P1800SCMC
Z2, Z3	2	58V, 500A Sidactor	Teccor Electronics	P0640SCMC
Z4, Z5	2	6V, 50A Sidactor	Teccor Electronics	P0080SAMC
Z9, Z10	2	25V, 500A Sidactor	Teccor Electronics	P0300SCMC

BASIC OPERATION

This design kit relies upon several supporting files, which can be downloaded from our website at www.maxim-ic.com/DS21354DK.

Hardware Configuration

Using the DK101 processor board:

- Connect the daughter card to the DK101 processor board.
- Supply 3.3V to the banana-plug receptacles marked GND and VCC_3.3V. (The external 5V connector and the TIM 5V supply headers are unused.)
- All processor board DIP switch settings should be in the ON position with exception for the flash programming switch, which should be OFF.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

Using the DK2000 processor board:

- Connect the daughter card to the DK2000 processor board.
- Connect J1 to the power supply that is delivered with the kit. Alternately, a PC power supply can be connected to connector J2.
- From the Programs menu launch the host application named ChipView.exe. Run the ChipView application. If the default installation options were used, click the Start button on the Windows toolbar and select Programs→ChipView→ChipView.

General:

- Upon power-up the RLOS LED is lit, as well as the MCLK-2.048MHz and TCLK-2.048MHz LEDs.
- Due to the dual winding transformer, only the 120Ω line build-out configuration setting is needed to cover 75Ω E1 and 120Ω E1.

Quick Setup (Demo Mode)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Demo Mode.
- The program requests a configuration file, then select DS21354_E1_DSNCOM_DRVR.cfg.
- The Demo Mode screen appears. Upon external loopback, the LOS and OOF indicators extinguish.

Quick Setup (Register View)

- The PC loads the program, offering a choice among Demo Mode, Register View, and Terminal Mode. Select Register View.
- The program requests a definition file, then select DS21354.def.
- The Register View screen appears, showing the register names, acronyms, and values. Note: During the definition file load process, all registers are initialized according to the init value filed in the definition file (because the SETUP field in the .def file is turned on).
- Predefined register settings for several functions are available as initialization files.
  - INI files are loaded by selecting the menu File→Reg Ini File→Load Ini File.
  - Load the INI file DS21354e1_fas_crc4_cas.ini.
  - After loading the INI file the following may be observed:

    The RLOS LED extinguishes upon external loopback.

    The device is now configured for E1 FAS with CRC4 and CAS.

Miscellaneous:

- Clock frequencies and certain pin bias levels are provided by a register-mapped CPLD, which is on the DS21354 daughter card.
- The definition file for this CPLD is named DS215x_35x_CPLD_V2.def. See the *CPLD Register Map* section for definitions.
- All files referenced above are available for download in the section marked “File Locations.”

REGISTER MAP

The DK101 daughter card address space begins at 0x81000000.
The DK2000 daughter card address space begins at:

0x30000000 for slot 0
0x40000000 for slot 1
0x50000000 for slot 2
0x60000000 for slot 3

All offsets given in Table 1 are relative to the beginning of the daughter card address space.

Table 1. Daughter Card Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0015	CPLD	Board identification and clock/signal routing
0X1000 to 0X10ff	Single-Chip Transceiver	Board is populated with one of the following: DS2155, DS2156, DS21352, or DS21354. Please see the data sheet(s) for details.

Registers in the CPLD can be easily modified using ChipView.exe, a host-based user interface software, along with the definition file named *DS215x_35x_CPLD_V2.def*. Definition files for the SCT are named *DS2155.def*, *DS21352.def*, or *DS21354.def*, depending on the board population option.

CPLD Register Map

Table 2. CPLD Register Map

OFFSET	NAME	TYPE	DESCRIPTION
0X0000	BID	Read-Only	Board ID
0X0002	XBIDH	Read-Only	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Board FAB Revision
0X0006	AREV	Read-Only	Board Assembly Revision
0X0007	PREV	Read-Only	PLD Revision
0X0011	SWITCH1	Read-Write	Pin to 1.544MHz
0X0012	SWITCH2	Read-Write	Pin to 2.048MHz
0X0013	SWITCH3	Read-Write	Pin-to-Pin Connect
0X0014	SWITCH4	Read-Write	Pin-to-Pin Connect
0X0015	LEVELS	Read-Write	Set Level On Pin 1 = 3.3V

ID Registers

OFFSET	NAME	TYPE	VALUE	DESCRIPTION
0X0000	BID	Read-Only	0xD	Board ID
0X0002	XBIDH	Read-Only	0x0	High-Nibble Extended Board ID
0X0003	XBIDM	Read-Only	0x0	Middle-Nibble Extended Board ID
0X0004	XBIDL	Read-Only	0x5	Low-Nibble Extended Board ID
0X0005	BREV	Read-Only	Displays current FAB revision	Board FAB Revision
0X0006	AREV	Read-Only	Displays current assembly revision	Board Assembly Revision
0X0007	PREV	Read-Only	Displays current PLD firmware revision	PLD Revision

Control Registers

The control registers are used primarily to control several banks of FET switches that route clocks and backplane signals. Please note that certain register settings cause line contention, e.g., setting SWITCH1.4 and SWITCH2.4 both to 0 would drive MCLK with both 1.544MHz and 2.048MHz.

SWITCH1: PIN TO 1.544MHz (OFFSET = 0x0011) INITIAL VALUE = 0xF

(MSB) **(LSB)**

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK

NAME	POSITION	FUNCTION
MCLK	SWITCH1.3	0 = Connect MCLK to the 1.544MHz clock 1 = Open Switch 1.4
TCLK	SWITCH1.2	0 = Connect TCLK to the 1.544MHz clock 1 = Open Switch 1.3
RSYSCLK	SWITCH1.1	0 = Connect RSYSCLK to the 1.544MHz clock 1 = Open Switch 1.2
TSYSCLK	SWITCH1.0	0 = Connect TSYSCLK to the 1.544MHz clock 1 = Open Switch 1.1

SWITCH2: PIN TO 2.048MHz (Offset = 0X0012) INITIAL VALUE = 0x3

(MSB) **(LSB)**

—	—	—	—	MCLK	TCLK	RSYSCLK	TSYSCLK

NAME	POSITION	FUNCTION
MCLK	SWITCH2.3	0 = Connect MCLK to the 2.048MHz clock 1 = Open Switch 2.4
TCLK	SWITCH2.2	0 = Connect TCLK to the 2.048MHz clock 1 = Open Switch 2.3
RSYSCLK	SWITCH2.1	0 = Connect RSYSCLK to the 2.048MHz clock 1 = Open Switch 2.2
TSYSCLK	SWITCH2.0	0 = Connect TSYSCLK to the 2.048MHz clock 1 = Open Switch 2.1

SWITCH3: PIN-TO-PIN CONNECT (Offset = 0X0013) INITIAL VALUE = 0xF

(MSB) **(LSB)**

—	—	—	—	TSS_RS	TCL_RC	RSY_RC	TSY_RC

NAME	POSITION	FUNCTION
TSS_RS	SWITCH3.3	0 = Connect TSSYNC to RSYNC 1 = Open Switch 3.4
TCL_RC	SWITCH3.2	0 = Connect TCLK to RCLK 1 = Open Switch 3.3
RSY_RC	SWITCH3.1	0 = Connect RSYSCLK to RCLK 1 = Open Switch 3.2
TSY_RC	SWITCH3.0	0 = Connect TSYSCLK to RCLK 1 = Open Switch 3.1

SWITCH4: PIN-TO-PIN CONNECT (Offset = 0X0014) INITIAL VALUE = 0x3

(MSB) **(LSB)**

—	—	—	—	URCLK_2048	UTCLK_2048	RSER_TSER	RSYNC_TSYNC

NAME	POSITION	FUNCTION
URCLK_2048	SWITCH4.3	0 = Connect UR_CLK (TSSYNC) to 2.048MHz 1 = Open Switch 4.4
UTCLK_2048	SWITCH4.2	0 = Connect UT_CLK (TCHCLK) to 2.048MHz 1 = Open Switch 4.3
RSER_TSER	SWITCH4.1	0 = Connect RER to TSER 1 = Open Switch 4.2
RSYNC_TSYNC	SWITCH4.0	0 = Connect RSYNC to TSYNC 1 = Open Switch 4.1

LEVELS: SET LEVEL ON PIN (Offset = 0X0015) INITIAL VALUE = 0x6

(MSB) **(LSB)**

—	—	—	—	—	BP_EN	PPCTDM_EN	TUSEL

NAME	POSITION	FUNCTION
—	LEVELS1.3	—
BP_EN	LEVELS1.2	0 = Enable IDT switches that connect the UTOPIA bus to daughter card header
PPCTDM_EN	LEVELS1.1	0 = Enable IDT switches that connect the TDM bus to the daughter card header
TUSEL	LEVELS1.0	0 = Set DS2156.TUSEL to enable TDM backplane 1 = Set DS2156.TUSEL to enable UTOPIA backplane

Note (DS2156 only): When the UTOPIA backplane is enabled (LEVELS.TUSEL = 1) there is a possibility for contention between the UTOPIA bus master and TSYSCLK, TSER, and RSER. To avoid this, the following switches should be opened when the UTOPIA backplane is enabled: SWITCH1.0, SWITCH2.0, SWITCH3.0, and SWITCH4.1

DS21354 INFORMATION

For more information about the DS21354, please consult the DS21354 data sheet available on our website at www.maxim-ic.com/DS21354. Software downloads are also available for this design kit.

DS21354DK INFORMATION

For more information about the DS21354DK, including software downloads, please consult the DS21354DK data sheet available on our website at www.maxim-ic.com/DS21354DK.

TECHNICAL SUPPORT

For additional technical support, please e-mail your questions to telecom.support@dalsemi.com.

SCHEMATICS

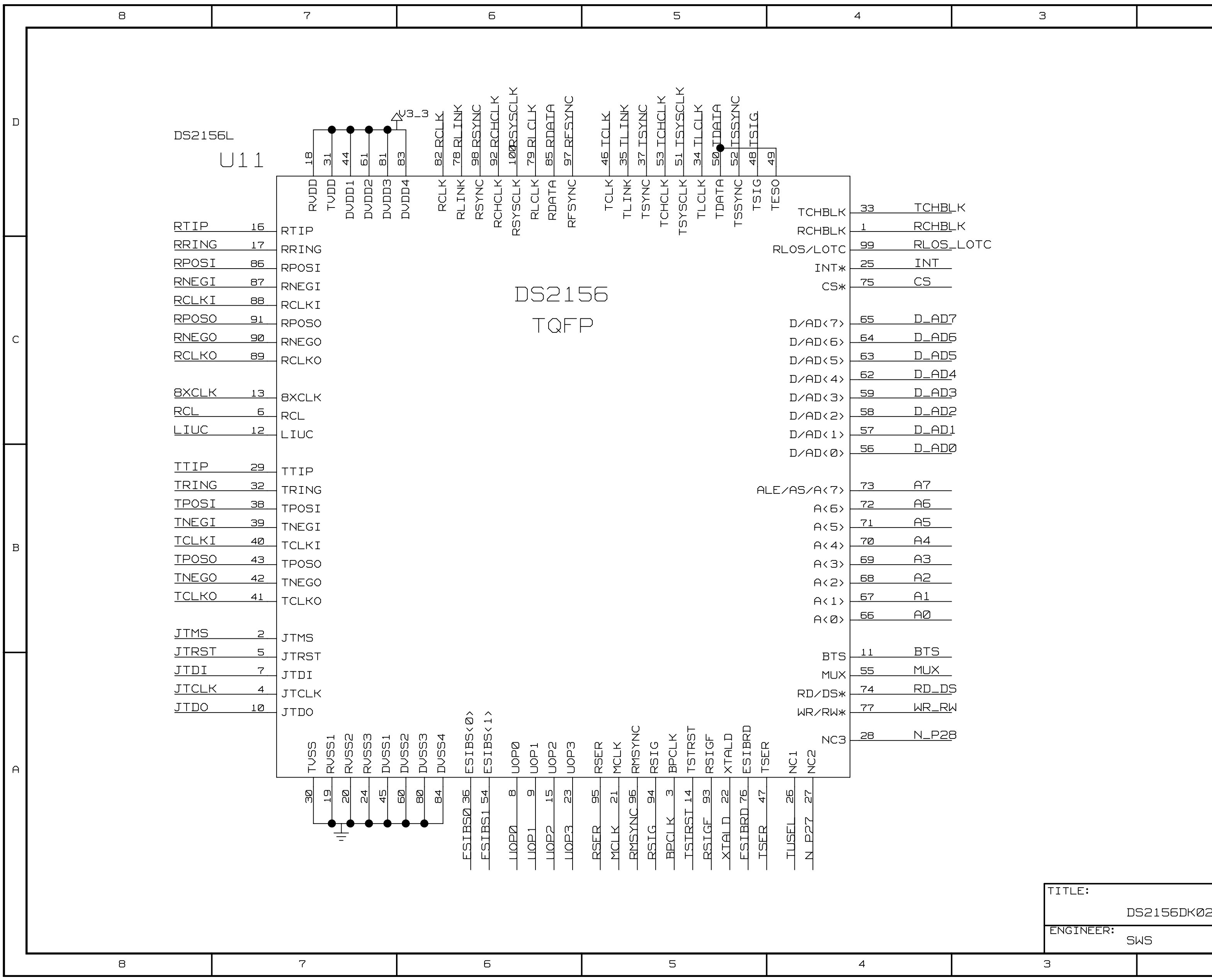
The DS21354DK schematics are featured in the following 13 pages.

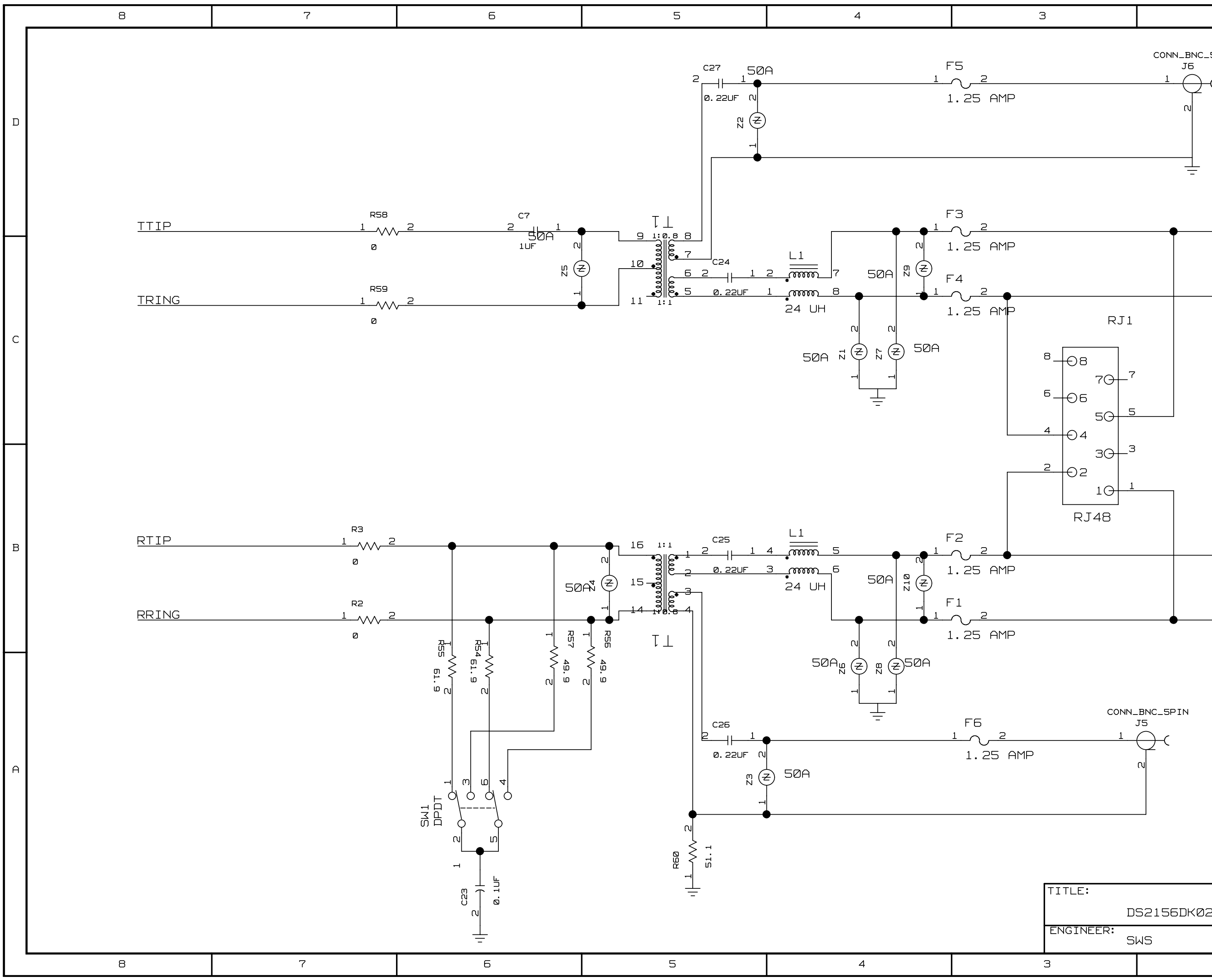
DS2156, DS2155, DS2135Y DESIGN

CONTENTS

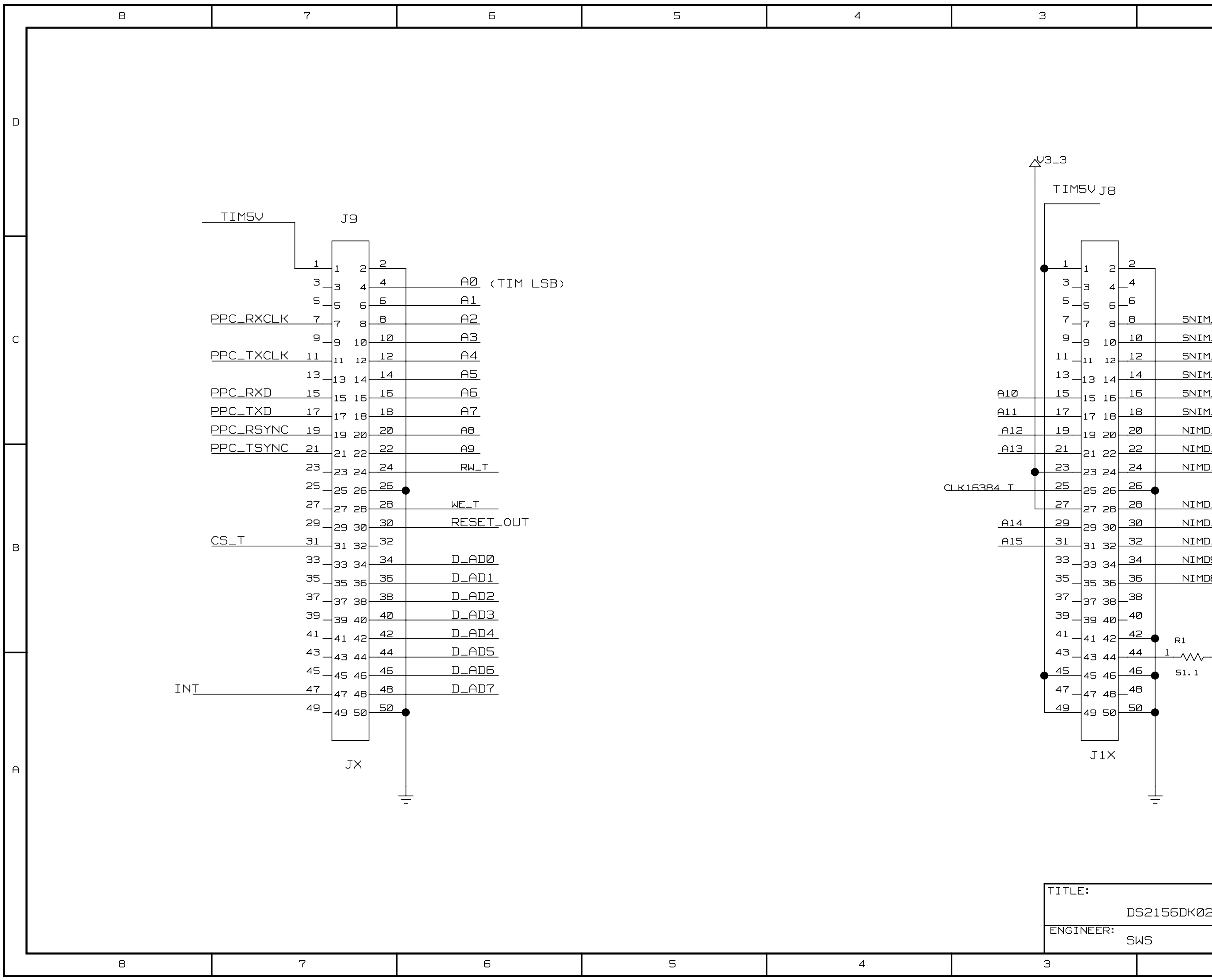
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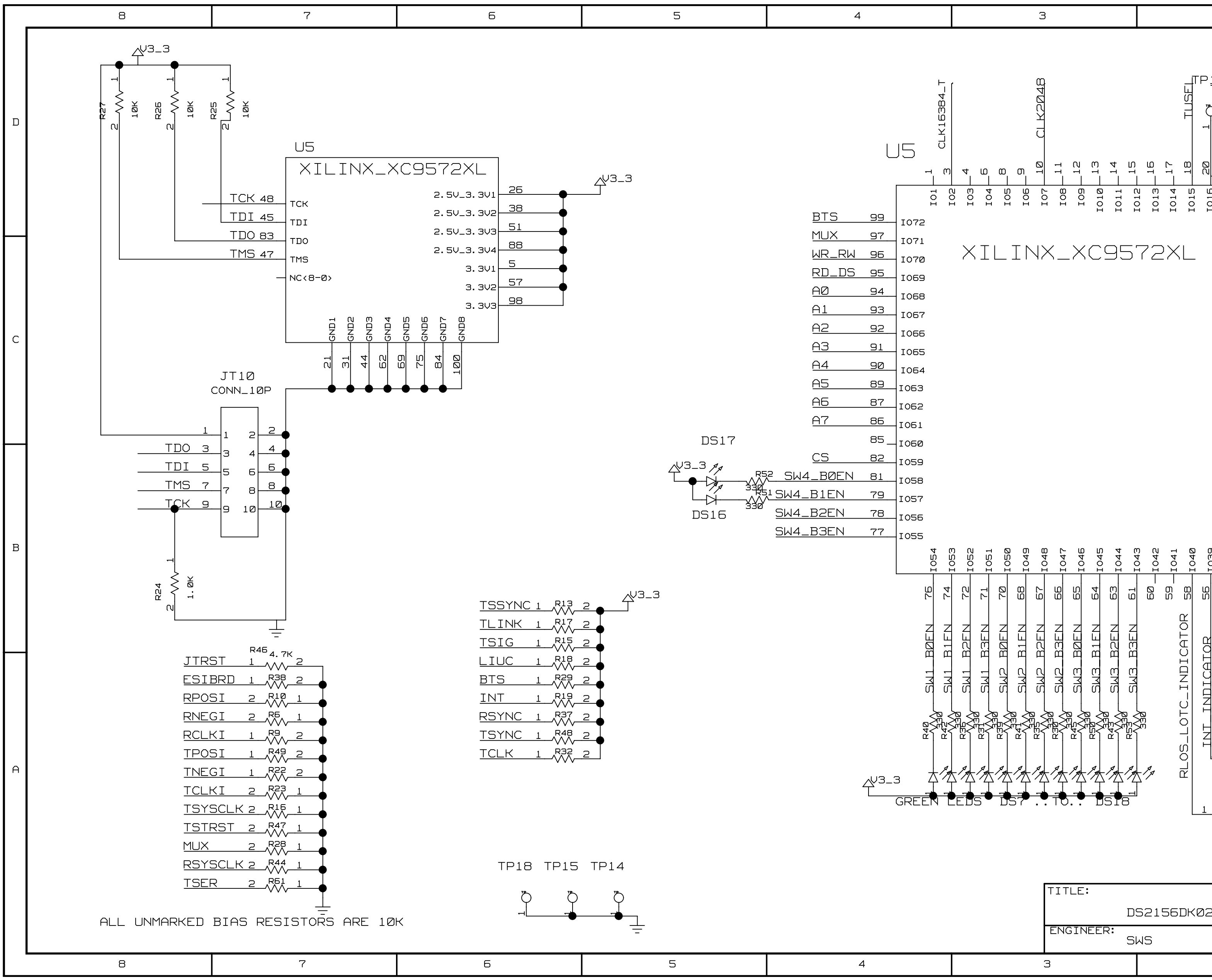

DS2156L
U11
DS2156
TQFP
V3_3
RVDD 18
TVDD 31
DVDD1 44
DVDD2 61
DVDD3 81
DVDD4 83
82 RCLK
78 RLINK
98 RSYNC
92 RCHCLK
100 RSYSCLK
79 RLCLK
85 RDATA
97 RFSYNC
46 TCLK
35 TLINK
37 TSYNC
53 TCHCLK
51 TSYSCLK
34 TLCLK
50 TDATA
52 TSSYNC
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49 TESO
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RRING 17
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RNEGO 90
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RCL 6
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TTIP 29
TRING 32
TPOSI 38
TNEGI 39
TCLKI 40
TPOSO 43
TNEGO 42
TCLKO 41
JTMS 2
JTRST 5
JTDI 7
JTCLK 4
JTDO 10
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RCHBLK 1 RCHBLK
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INT* 25 INT
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D/AD<7> 65 D_AD7
D/AD<6> 64 D_AD6
D/AD<5> 63 D_AD5
D/AD<4> 62 D_AD4
D/AD<3> 59 D_AD3
D/AD<2> 58 D_AD2
D/AD<1> 57 D_AD1
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ALE/AS/A<7> 73 A7
A<6> 72 A6
A<5> 71 A5
A<4> 70 A4
A<3> 69 A3
A<2> 68 A2
A<1> 67 A1
A<0> 66 A0
BTS 11 BTS
MUX 55 MUX
RD/DS* 74 RD_DS
WR/RW* 77 WR_RW
NC3 28 N_P28
TVSS 30
RVSS1 19
RVSS2 20
RVSS3 24
DVSS1 45
DVSS2 60
DVSS3 80
DVSS4 84
ESIBS<0> 36 ESIBS0
ESIBS<1> 54 ESIBS1
UOP0 8 UOP0
UOP1 9 UOP1
UOP2 15 UOP2
UOP3 23 UOP3
RSER 95 RSER
MCLK 21 MCLK
RMSYNC 96 RMSYNC
RSIG 94 RSIG
BPCLK 3 BPCLK
TSTRST 14 TSTRST
RSIGF 93 RSIGF
XTALD 22 XTALD
ESIBRD 76 ESIBRD
TSER 47 TSER
NC1 26 TUSEL
NC2 27 N_P27
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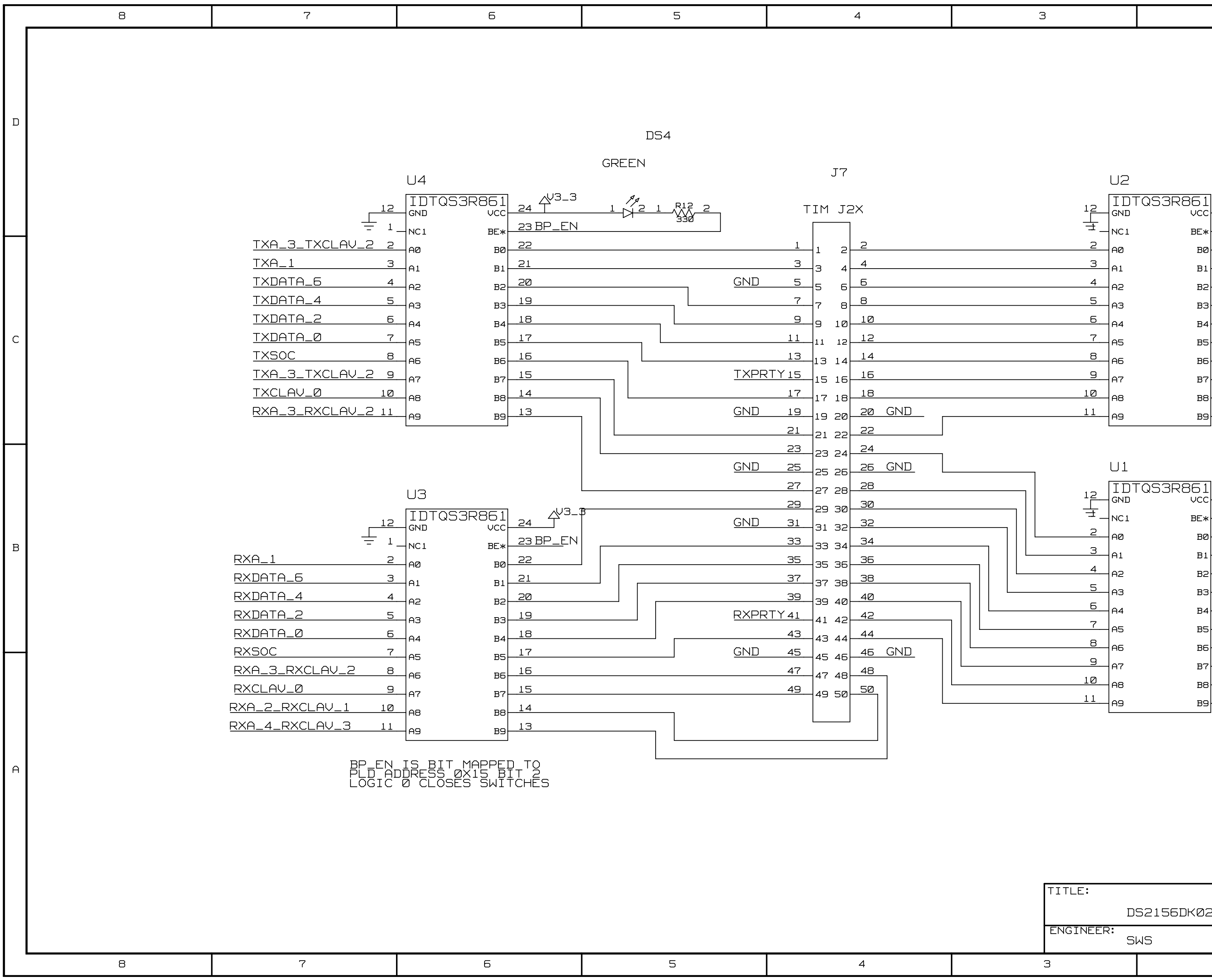
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RRING
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R59
R3
R2
R55
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R56
R60
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C25
C26
C27
T1
L1
24 UH
F1
F2
F3
F4
F5
F6
1.25 AMP
Z1
Z2
Z3
Z4
Z5
Z6
Z7
Z8
Z9
Z10
50A
0.22UF
1UF
0.1UF
61.9
49.9
51.1
SW1
DPDT
RJ1
RJ48
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J6
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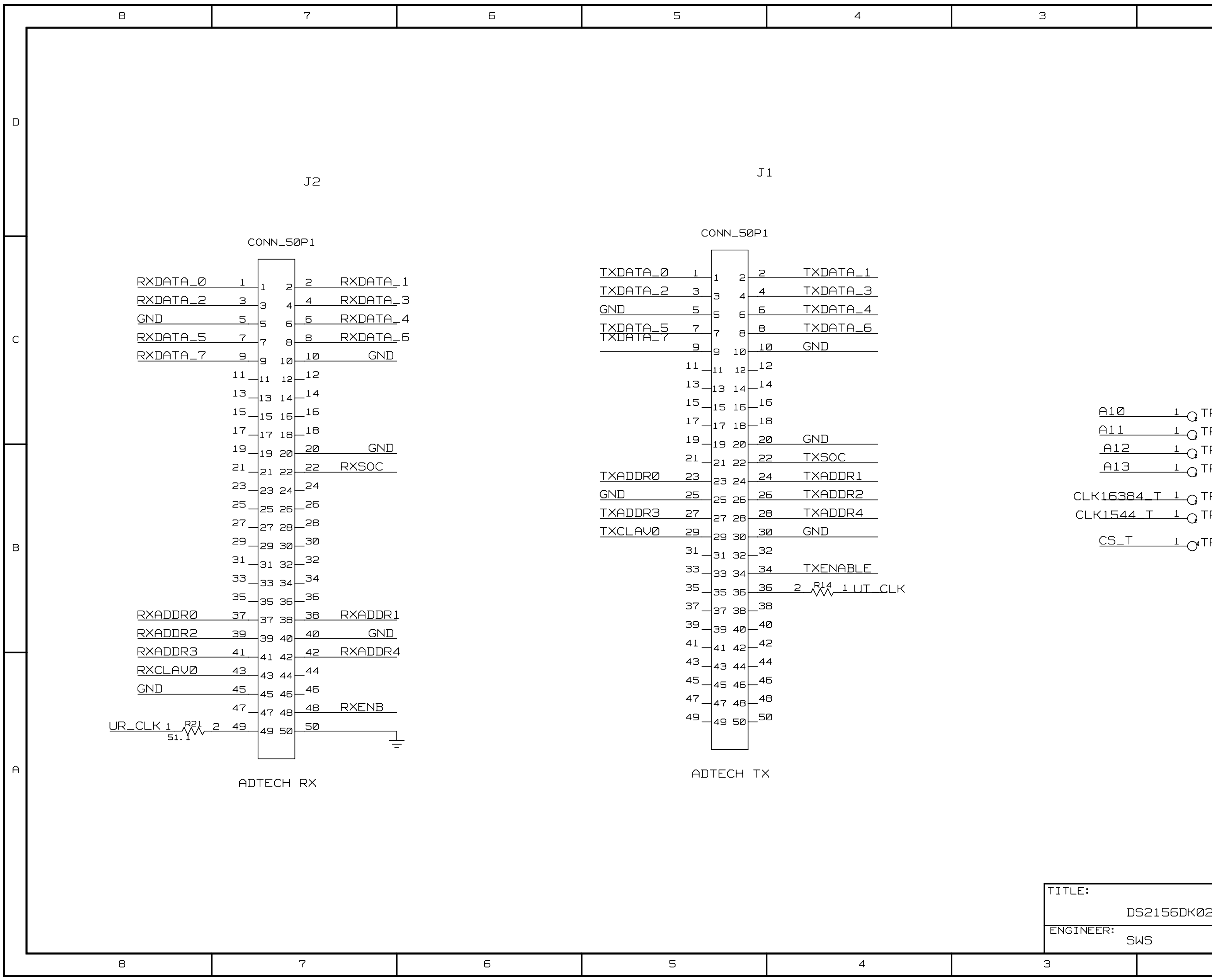


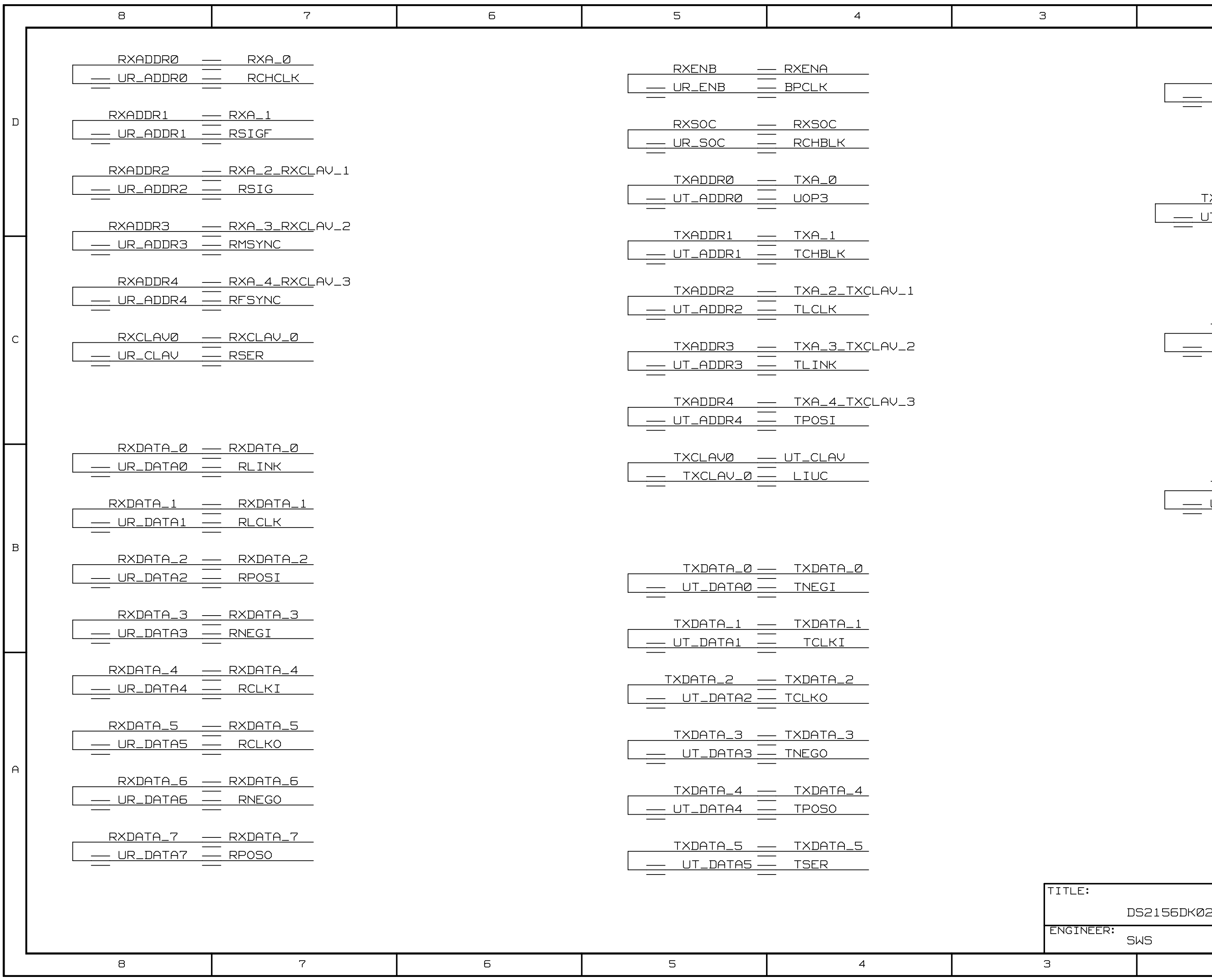
TIM5V
J9
PPC_RXCLK
PPC_TXCLK
PPC_RXD
PPC_TXD
PPC_RSYNC
PPC_TSYNC
CS_T
INT
A0 (TIM LSB)
A1
A2
A3
A4
A5
A6
A7
A8
A9
RW_T
WE_T
RESET_OUT
D_AD0
D_AD1
D_AD2
D_AD3
D_AD4
D_AD5
D_AD6
D_AD7
JX
V3_3
TIM5V
J8
A10
A11
A12
A13
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51.1
J1X
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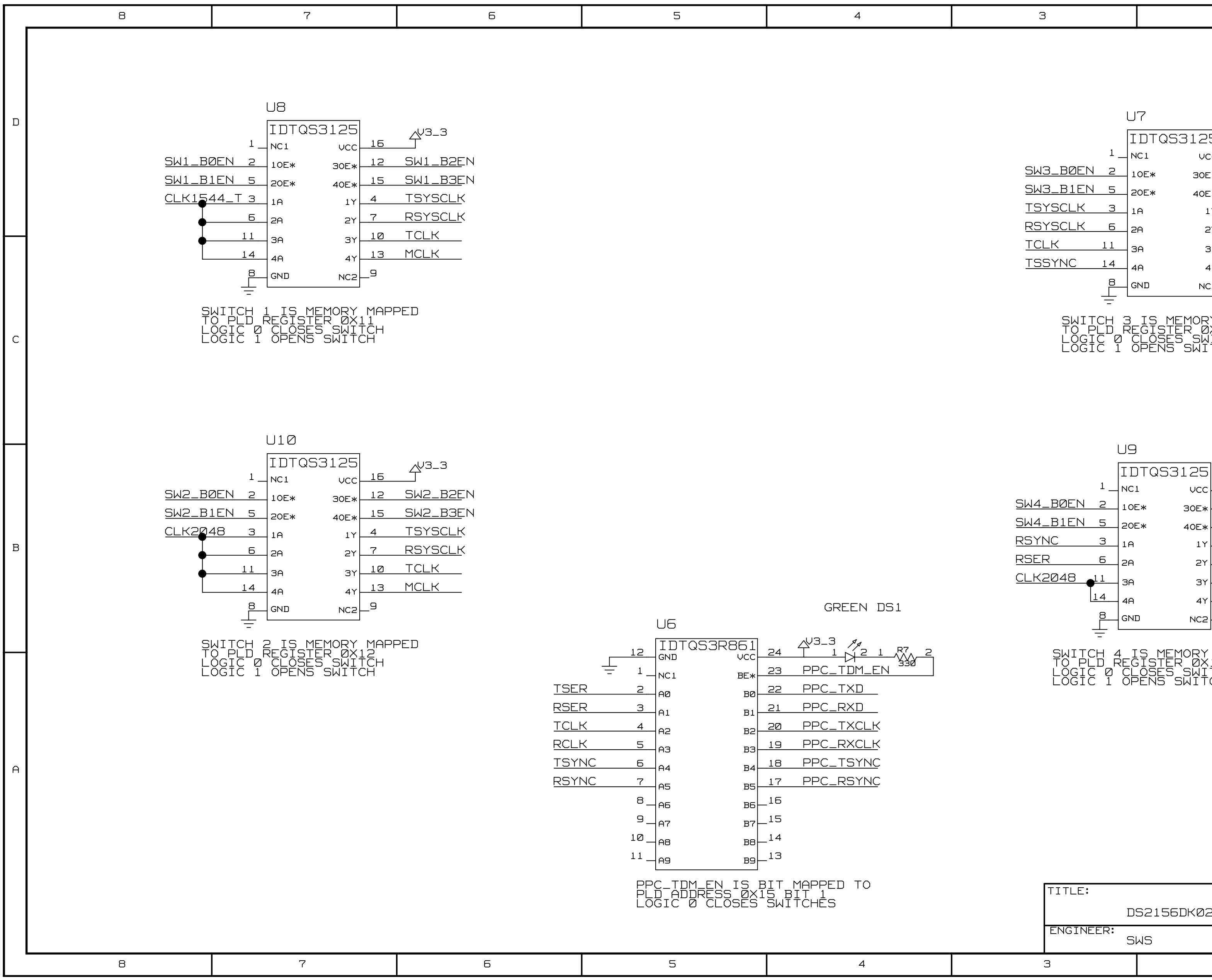
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3.3V2
3.3V3
V3_3
R27
R26
R25
10K
JT10
CONN_10P
R24
1.0K
DS17
DS16
BTS
MUX
WR_RW
RD_DS
A0
A1
A2
A3
A4
A5
A6
A7
CS
SW4_B0EN
SW4_B1EN
SW4_B2EN
SW4_B3EN
CLK16384_T
CLK2048
TUSEL
SW1_B0EN
SW1_B1EN
SW1_B2EN
SW1_B3EN
SW2_B0EN
SW2_B1EN
SW2_B2EN
SW2_B3EN
SW3_B0EN
SW3_B1EN
SW3_B2EN
SW3_B3EN
RLOS_LOTC_INDICATOR
INT_INDICATOR
GREEN LEDS DS7 ..TO.. DS18
TSSYNC
TLINK
TSIG
LIUC
BTS
INT
RSYNC
TSYNC
TCLK
JTRST
ESIBRD
RPOSI
RNEGI
RCLKI
TPOSI
TNEGI
TCLKI
TSYSCLK
TSTRST
MUX
RSYSCLK
TSER
R46 4.7K
TP18 TP15 TP14
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ENGINEER:
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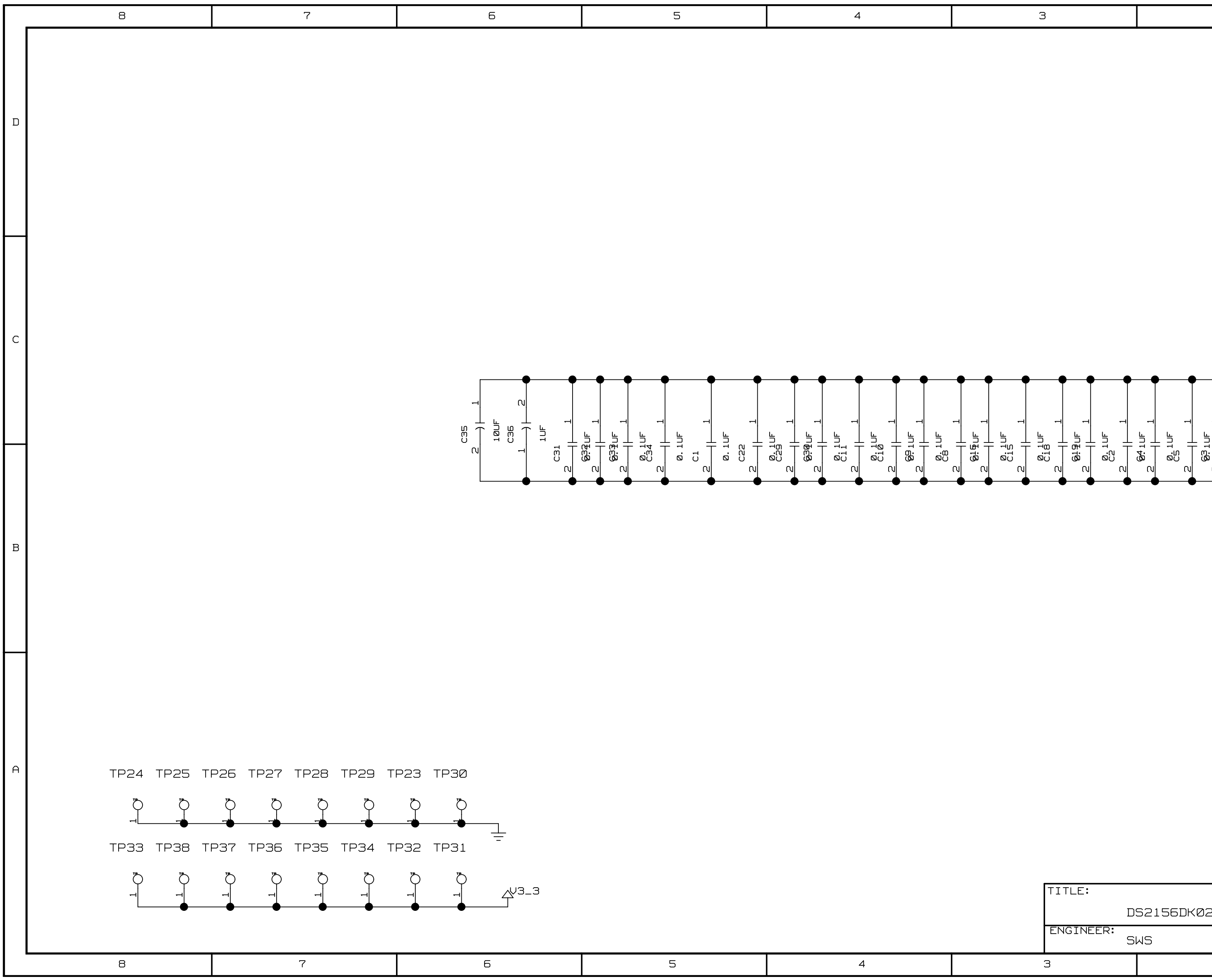

DS4
GREEN
R12
330
J7
TIM J2X
U4
IDTQS3R861
U3
IDTQS3R861
U2
IDTQS3R861
U1
IDTQS3R861
V3_3
BP_EN
TXA_3_TXCLAV_2
TXA_1
TXDATA_6
TXDATA_4
TXDATA_2
TXDATA_0
TXSOC
TXCLAV_0
RXA_3_RXCLAV_2
RXA_1
RXDATA_6
RXDATA_4
RXDATA_2
RXDATA_0
RXSOC
RXCLAV_0
RXA_2_RXCLAV_1
RXA_4_RXCLAV_3
TXPRTY
RXPRTY
GND
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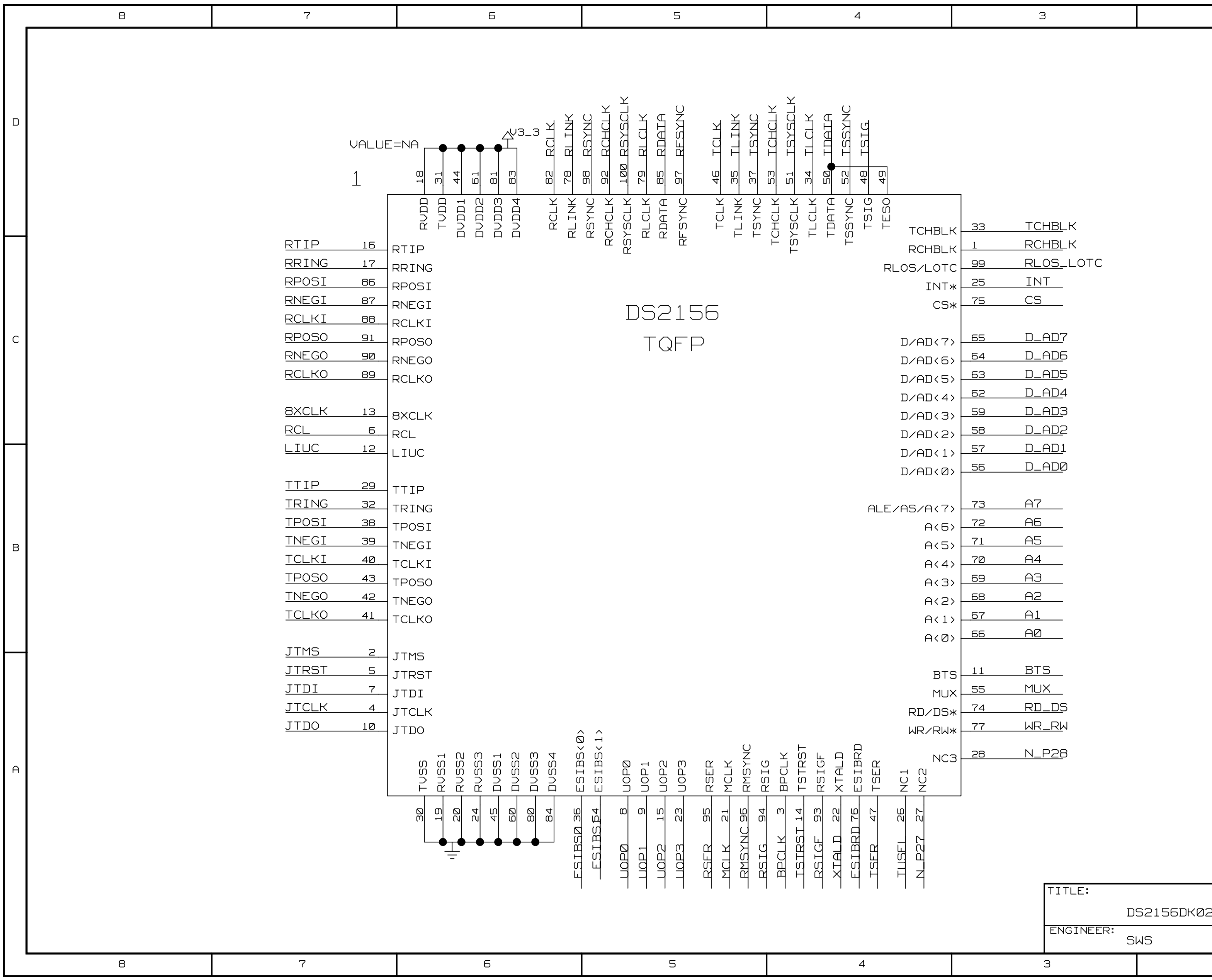

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CONN_50P1
RXDATA_0
RXDATA_1
RXDATA_2
RXDATA_3
GND
RXDATA_4
RXDATA_5
RXDATA_6
RXDATA_7
GND
GND
RXSOC
RXADDR0
RXADDR1
RXADDR2
GND
RXADDR3
RXADDR4
RXCLAV0
GND
RXENB
UR_CLK
R21
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TXDATA_2
TXDATA_3
GND
TXDATA_4
TXDATA_5
TXDATA_6
TXDATA_7
GND
GND
TXSOC
TXADDR0
TXADDR1
GND
TXADDR2
TXADDR3
TXADDR4
TXCLAV0
GND
TXENABLE
R14
UT_CLK
ADTECH TX
A10
A11
A12
A13
CLK16384_T
CLK1544_T
CS_T
TITLE:
DS2156DK02
ENGINEER:
SWS



RXADDR0 RXA_0
UR_ADDR0 RCHCLK
RXADDR1 RXA_1
UR_ADDR1 RSIGF
RXADDR2 RXA_2_RXCLAV_1
UR_ADDR2 RSIG
RXADDR3 RXA_3_RXCLAV_2
UR_ADDR3 RMSYNC
RXADDR4 RXA_4_RXCLAV_3
UR_ADDR4 RFSYNC
RXCLAV0 RXCLAV_0
UR_CLAV RSER
RXDATA_0 RXDATA_0
UR_DATA0 RLINK
RXDATA_1 RXDATA_1
UR_DATA1 RLCLK
RXDATA_2 RXDATA_2
UR_DATA2 RPOSI
RXDATA_3 RXDATA_3
UR_DATA3 RNEGI
RXDATA_4 RXDATA_4
UR_DATA4 RCLKI
RXDATA_5 RXDATA_5
UR_DATA5 RCLKO
RXDATA_6 RXDATA_6
UR_DATA6 RNEGO
RXDATA_7 RXDATA_7
UR_DATA7 RPOSO
RXENB RXENA
UR_ENB BPCLK
RXSOC RXSOC
UR_SOC RCHBLK
TXADDR0 TXA_0
UT_ADDR0 UOP3
TXADDR1 TXA_1
UT_ADDR1 TCHBLK
TXADDR2 TXA_2_TXCLAV_1
UT_ADDR2 TLCLK
TXADDR3 TXA_3_TXCLAV_2
UT_ADDR3 TLINK
TXADDR4 TXA_4_TXCLAV_3
UT_ADDR4 TPOSI
TXCLAV0 UT_CLAV
TXCLAV_0 LIUC
TXDATA_0 TXDATA_0
UT_DATA0 TNEGI
TXDATA_1 TXDATA_1
UT_DATA1 TCLKI
TXDATA_2 TXDATA_2
UT_DATA2 TCLKO
TXDATA_3 TXDATA_3
UT_DATA3 TNEGO
TXDATA_4 TXDATA_4
UT_DATA4 TPOSO
TXDATA_5 TXDATA_5
UT_DATA5 TSER
TITLE:
DS2156DK02
ENGINEER:
SWS


U8
IDTQS3125
SW1_B0EN
SW1_B1EN
CLK1544_T
V3_3
SW1_B2EN
SW1_B3EN
TSYSCLK
RSYSCLK
TCLK
MCLK
SWITCH 1 IS MEMORY MAPPED
TO PLD REGISTER 0X11
LOGIC 0 CLOSES SWITCH
LOGIC 1 OPENS SWITCH
U10
IDTQS3125
SW2_B0EN
SW2_B1EN
CLK2048
SW2_B2EN
SW2_B3EN
TSYSCLK
RSYSCLK
TCLK
MCLK
SWITCH 2 IS MEMORY MAPPED
TO PLD REGISTER 0X12
LOGIC 0 CLOSES SWITCH
LOGIC 1 OPENS SWITCH
U7
IDTQS3125
SW3_B0EN
SW3_B1EN
TSYSCLK
RSYSCLK
TCLK
TSSYNC
U9
IDTQS3125
SW4_B0EN
SW4_B1EN
RSYNC
RSER
CLK2048
GREEN DS1
U6
IDTQS3R861
TSER
RSER
TCLK
RCLK
TSYNC
RSYNC
PPC_TDM_EN
PPC_TXD
PPC_RXD
PPC_TXCLK
PPC_RXCLK
PPC_TSYNC
PPC_RSYNC
R7
330
PPC_TDM_EN IS BIT MAPPED TO
PLD ADDRESS 0X15 BIT 1
LOGIC 0 CLOSES SWITCHES
TITLE:
DS2156DK02
ENGINEER:
SWS


8
7
6
5
4
3
D
C
B
A
C35
10UF
C36
1UF
C31
C34
C1
C22
C29
C11
C10
C8
C15
C18
C2
C5
0.1UF
TP24 TP25 TP26 TP27 TP28 TP29 TP23 TP30
TP33 TP38 TP37 TP36 TP35 TP34 TP32 TP31
V3_3
TITLE:
DS2156DK02
ENGINEER:
SWS



VALUE=NA
V3_3
1
DS2156
TQFP
RVDD
TVDD
DVDD1
DVDD2
DVDD3
DVDD4
RCLK
RLINK
RSYNC
RCHCLK
RSYSCLK
RLCLK
RDATA
RFSYNC
TCLK
TLINK
TSYNC
TCHCLK
TSYSCLK
TLCLK
TDATA
TSSYNC
TSIG
TESO
RTIP
RRING
RPOSI
RNEGI
RCLKI
RPOSO
RNEGO
RCLKO
8XCLK
RCL
LIUC
TTIP
TRING
TPOSI
TNEGI
TCLKI
TPOSO
TNEGO
TCLKO
JTMS
JTRST
JTDI
JTCLK
JTDO
TCHBLK
RCHBLK
RLOS/LOTC
RLOS_LOTC
INT*
INT
CS*
CS
D/AD<7> D_AD7
D/AD<6> D_AD6
D/AD<5> D_AD5
D/AD<4> D_AD4
D/AD<3> D_AD3
D/AD<2> D_AD2
D/AD<1> D_AD1
D/AD<0> D_AD0
ALE/AS/A<7> A7
A<6> A6
A<5> A5
A<4> A4
A<3> A3
A<2> A2
A<1> A1
A<0> A0
BTS
MUX
RD/DS* RD_DS
WR/RW* WR_RW
NC3 N_P28
TVSS
RVSS1
RVSS2
RVSS3
DVSS1
DVSS2
DVSS3
DVSS4
ESIBS<0> ESIBS0
ESIBS<1> ESIBS1
UOP0
UOP1
UOP2
UOP3
RSER
MCLK
RMSYNC
RSIG
BPCLK
TSTRST
RSIGF
XTALD
ESIBRD
TSER
NC1 TUSEL
NC2 N_P27
TITLE:
DS2156DK02
ENGINEER:
SWS

```
*** Signal Cross-Reference for the entire design ***

8XCLK              2C8> 11C7>
A0                 4C6<> 5C4<> 2B3< 11B3<
A1                 4C6<> 5C4<> 2B3< 11B3<
A2                 4C6<> 5C4<> 2B3< 11B3<
A3                 4C6<> 5C4<> 2B3< 11B3<
A4                 4C6<> 5C4<> 2B3< 11B3<
A5                 4C6<> 5C4<> 2B3< 11B3<
A6                 4C6<> 5C4<> 2B3< 11B3<
A7                 4C6<> 5C4<> 2B3< 11B3<
A8                 4C6<> 7B1<>
A9                 4B6<> 7B1<>
A10                4C3<> 7C3<>
A11                4C3<> 5C1<> 7C3<>
A12                4C3<> 5C1<> 7B3<>
A13                4B3<> 7B3<>
A14                4B3<>
A15                4B3<>
BPCLK              2A5> 8D4> 11A4>
BP_EN              5C1<> 6B2< 6B6< 6C2< 6C6<
BTS                5D4<> 2B3< 5A6< 11A3<
CLK1544_T          7B3<> 9D8<> 4B2<
CLK2048            5D3<> 9B3<> 9B8<>
CLK16384_T         4B4<> 5D3<> 7B3<>
CS                 5B4<> 2C3< 11C3<
CS_T               4B8<> 5B1<> 7B3<>
D_AD0              2B3<> 4B6<> 5C1<> 11B3<>
D_AD1              2C3<> 4B6<> 5C1<> 11B3<>
D_AD2              2C3<> 4B6<> 5C1<> 11C3<>
D_AD3              2C3<> 4B6<> 5C1<> 11C3<>
D_AD4              2C3<> 4B6<> 5C1<> 11C3<>
D_AD5              2C3<> 4B6<> 5C1<> 11C3<>
D_AD6              2C3<> 4A6<> 5C1<> 11C3<>
D_AD7              2C3<> 4A6<> 5D1<> 11C3<>
ESIBRD             2A5<> 11A4<> 5A8<
ESIBS0             2A6<> 11A6<>
ESIBS1             2A6<> 11A5<>
INT                2C3> 4A8<> 5A2<> 11C3> 5A6<
INT_INDICATOR      5A2<>
JTCLK              2A8< 11A7<
JTDI               2A8< 11A7<
JTDO               2A8> 11A7>
JTMS               2B8< 11B7<
JTRST              2B8< 5A8< 11A7<
LIUC               8B4> 2C8< 5A6< 11B7<
MCLK               9B6<> 9C6<> 2A5< 11A5<
MUX                5C4<> 2A3< 5A8< 11A3<
NIMD8              4B2<>
NIMD9              4B2<>
NIMD10             4B2<>
NIMD11             4B2<>
NIMD12             4B2<>
NIMD13             4B2<>
NIMD14             4B2<>
NIMD15             4C2<>
N_P27              2A4< 11A4<
N_P28              2A3< 11A3<
PPC_RSYNC          4C8<> 9A4<>
PPC_RXCLK          4C8<> 9A4<>
PPC_RXD            4C8<> 9A4<>
PPC_TDM_EN         5C1<> 9A4<
PPC_TSYNC          4B8<> 9A4<>
PPC_TXCLK          4C8<> 9A4<>
PPC_TXD            4C8<> 9A4<>
RCHBLK             2C3> 8D4> 11C3>
RCHCLK             2D6> 8D7> 11D5>
RCL                2C8> 11C7>
RCLK               2D6> 9A6<> 9C1<> 9C1<> 9D1<> 11D6>

RCLKI              8A7> 2C8< 5A8< 11C7<
RCLKO              2C8> 8A7> 11C7>
RDATA              2D6> 11D5>
RD_DS              5C4<> 2A3< 11A3<
RESET_OUT          4B6<> 5B1<> 7B1<>
RFSYNC             2D6> 8C7> 11D5>
RLCLK              2D6> 8B7> 11D5>

RLINK              2D6> 8B7> 11D6>
RLOS_LOTC          2C3> 5B2<> 11C3>
RLOS_LOTC_INDICATOR  5A2<>
RMSYNC             2A5> 8C7> 11A5>
RNEGI              8B7> 2C8< 5A8< 11C7<
RNEGO              2C8> 8A7> 11C7>
RPOSI              8B7> 2C8< 5A8< 11C7<
RPOSO              2C8> 8A7> 11C7>
RRING              2C8< 3B8< 11C7<
RSER               2A5> 8C7> 9A6<> 9B3<> 11A5>
RSIG               2A5> 8D7> 11A5>
RSIGF              2A5> 8D7> 11A4>
RSYNC              2D6<> 9A6<> 9B3<> 9C1<> 11D5<>
                 5A6<
RSYSCLK            9B6<> 9C3<> 9D6<> 2D6< 5A8< 11D5<
RTIP               2C8< 3B8< 11C7<
RW_T               4B6<> 5B1<> 7B1<>
RXADDR0            7B8<> 8D8
RXADDR1            7B6<> 8D8
RXADDR2            7B8<> 8D8
RXADDR3            7B8<> 8C8
RXADDR4            7B6<> 8C8
RXA_0              6B2<> 8D7>
RXA_1              6B7<> 8D7>
RXA_2_RXCLAV_1     6A7<> 6B2<> 8D7>
RXA_3_RXCLAV_2     6A7<> 6C7<> 8C7>
RXA_4_RXCLAV_3     6A7<> 6B2<> 8C7>
RXCLAV0            7A8<> 8C8
RXCLAV_0           6A7<> 8C7>
RXDATA_0           6B7<> 7C8<> 8B7> 8B8
RXDATA_1           6A2<> 7C6<> 8B7> 8B8
RXDATA_2           6B7<> 7C8<> 8B7> 8B8
RXDATA_3           6B2<> 7C6<> 8B7> 8B8
RXDATA_4           6B7<> 7C6<> 8A7> 8A8
RXDATA_5           6B2<> 7C8<> 8A7> 8A8
RXDATA_6           6B7<> 7C6<> 8A7> 8A8
RXDATA_7           6B2<> 7C8<> 8A7> 8A8
RXENA              6A2<> 8D4>
RXENB              7A6<> 8D5
RXPRTY             6B5<>
RXSOC              6B7<> 7B6<> 8D4> 8D5
SNIM_B2            4C2<>
SNIM_B3            4C2<>
SNIM_B4            4C2<>
SNIM_B5            4C2<>
SNIM_B6            4C2<>
SNIM_B7            4C2<>
SW1_B0EN           5A4<> 9D8<
SW1_B1EN           5A4<> 9D8<
SW1_B2EN           5A3<> 9D6<
SW1_B3EN           5A3<> 9D6<
SW2_B0EN           5A3<> 9B8<
SW2_B1EN           5A3<> 9B8<
SW2_B2EN           5A3<> 9B6<
SW2_B3EN           5A3<> 9B6<
SW3_B0EN           5A3<> 9D3<
SW3_B1EN           5A3<> 9D3<
SW3_B2EN           5A3<> 9D1<
SW3_B3EN           5A3<> 9D1<
SW4_B0EN           5B4<> 9B3<
SW4_B1EN           5B4<> 9B3<
SW4_B2EN           5B4<> 9B2<
SW4_B3EN           5B4<> 9B2<
TCHBLK             2D3> 8C4> 11C3>
TCHCLK             2D5> 11D4> 8A1<
TCK                5B8<> 5D8<
TCLK               9A6<> 9B6<> 9C3<> 9C6<> 2D5< 5A6<
                 11D5<
TCLKI              8B4> 2B8< 5A8< 11B7<
TCLKO              2B8> 8A4> 11B7>
TDATA              2D5<> 11D4<>
TDI                5B8<> 5D7<
TDO                5B8<> 5C7<
TIM5V              4D3<> 4D8<>
TLCLK              2D5> 8C4> 11D4>
TLINK              8C4> 2D5< 5B6< 11D5<
TMS                5B8<> 5C7<

TNEGI              8B4> 2B8< 5A8< 11B7<
TNEGO              2B8> 8A4> 11B7>
TPOSI              8C4> 2B8< 5A8< 11B7<
TPOSO              2B8> 8A4> 11B7>
TRING              2B8> 11B7> 3C8<
TSER               8A4> 9A6<> 9B2<> 2A5< 5A8< 11A4<
TSIG               8D1> 2D5< 5B6< 11D4<
TSSYNC             9C3<> 2D5< 5B6< 8A1< 11D4<
TSTRST             2A5< 5A8< 11A4<
TSYNC              2D5<> 9A6<> 9B2<> 11D5<> 5A6<
TSYSCLK            8D1> 9B6<> 9D3<> 9D6<> 2D5< 5A8<
                 11D4<
TTIP               2B8> 11B7> 3C8<
TUSEL              5D2<> 2A4< 11A4<
TXADDR0            7B5<> 8D5
TXADDR1            7B4<> 8C5
TXADDR2            7B4<> 8C5
TXADDR3            7B5<> 8C5
TXADDR4            7B4<> 8C5
TXA_0              6C2<> 8D4>
TXA_1              6C7<> 8C4>
TXA_2_TXCLAV_1     6B2<> 6C2<> 8C4>
TXA_3_TXCLAV_2     6C7<> 6C7<> 8C4>
TXA_4_TXCLAV_3     6C2<> 6C2<> 8C4>
TXCLAV0            7B5<> 8B5
TXCLAV_0           6C7<> 8B5
TXDATA_0           6C7<> 7C5<> 8B4> 8B5
TXDATA_1           6C2<> 7C4<> 8B4> 8B5
TXDATA_2           6C7<> 7C5<> 8A4> 8A5
TXDATA_3           6C2<> 7C4<> 8A4> 8A5
TXDATA_4           6C7<> 7C4<> 8A4> 8A5
TXDATA_5           6C2<> 7C5<> 8A4> 8A5
TXDATA_6           6C7<> 7C4<> 8D1> 8D2
TXDATA_7           6C2<> 7C5<> 8D1> 8D2
TXENA              6C2<> 8C1>
TXENABLE           7B4<> 8C2
TXPRTY             6C5<>
TXSOC              6C7<> 7B4<> 8B1> 8B2
UOP0               2A6> 8B1> 11A5>
UOP1               2A6> 8C1> 11A5>
UOP2               2A6> 11A5>
UOP3               2A6> 8D4> 11A5>
UR_ADDR0           8D8
UR_ADDR1           8D8
UR_ADDR2           8D8
UR_ADDR3           8C8
UR_ADDR4           8C8
UR_CLAV            8C8
UR_CLK             9B2<> 6A1< 7A8< 8A2<
UR_DATA0           8B8
UR_DATA1           8B8
UR_DATA2           8B8
UR_DATA3           8B8
UR_DATA4           8A8
UR_DATA5           8A8
UR_DATA6           8A8
UR_DATA7           8A8
UR_ENB             8D5
UR_SOC             8D5
UT_ADDR0           8D5
UT_ADDR1           8C5
UT_ADDR2           8C5
UT_ADDR3           8C5
UT_ADDR4           8C5
UT_CLAV            8B4>
UT_CLK             9B2<> 6C1< 7B4< 8A2<
UT_DATA0           8B5
UT_DATA1           8B5
UT_DATA2           8A5
UT_DATA3           8A5
UT_DATA4           8A5
UT_DATA5           8A5
UT_DATA6           8D2
UT_DATA7           8D2
UT_ENB             8C2
UT_SOC             8B2
WE_T               4B6<> 5B1<> 7B1<>

WR_RW              5C4<> 2A3<
XTALD              2A5> 11A4>
```

TITLE: DS2156DK02

ENGINEER: SWS

*** Part Cross-Reference for the entire design ***

1	DS2156_TQFP	11D7
C1	CAP	10B5
C2	CAP	10B3
C3	CAP	10B2
C4	CAP	10B2
C5	CAP	10B2
C7	CAP	3D6
C8	CAP	10B4
C9	CAP	10B4
C10	CAP	10B4
C11	CAP	10B4
C12	CAP	10B2
C13	CAP	8A1
C14	CAP	8A1
C15	CAP	10B3
C16	CAP	10B3
C17	CAP	10B2
C18	CAP	10B3
C19	CAP	10B3
C21	CAP	10B2
C22	CAP	10B5
C23	CAP	3A6
C24	CAP	3C5
C25	CAP	3B5
C26	CAP	3A5
C27	CAP	3D5
C29	CAP	10B4
C30	CAP	10B4
C31	CAP	10B6
C32	CAP	10B5
C33	CAP	10B5
C34	CAP	10B5
C35	CAP	10B6
C36	CAP	10B6
DS1	LED	9B4
DS2	LED	5A2
DS3	LED	5A2
DS4	LED	6D5
DS5	LED	5A3
DS6	LED	5A4
DS7	LED	5A3
DS8	LED	5A4
DS9	LED	5A4
DS10	LED	5A3
DS11	LED	5A4
DS12	LED	5A3
DS13	LED	5A3
DS14	LED	5A3
DS15	LED	5A3
DS16	LED	5B5
DS17	LED	5B5
DS18	LED	5A3
F1	FUSE	3B4
F2	FUSE	3B4
F3	FUSE	3D4
F4	FUSE	3C4
F5	FUSE	3D4
F6	FUSE	3A3
J1	CONN_50P1	7D5
J2	CONN_50P1	7D7
J3	CONN_BANTAM_IPC	3B1
J4	CONN_BANTAM_IPC	3C1
J5	CONN_BNC_5PIN	3A3
J6	CONN_BNC_5PIN	3D2
J7	CONN_50P2	6D4
J8	CONN_50P2	4D3
J9	CONN_50P2	4D7
JT10	CONN_10P	5C8
L1	CHOKE_DUAL_T1	3B4 3C4
R1	RES1	4B2
R2	RES	3B7
R3	RES	3B7
R4	RES	6A2
R5	RES	6C2
R6	RES1	5A7
R7	RES	9B4
R8	RES1	5A2
R9	RES1	5A7
R10	RES1	5A7
R11	RES1	5A2
R12	RES	6D5
R13	RES1	5B6
R14	RES1	7B4
R15	RES1	5B6
R16	RES1	5A7
R17	RES1	5B6
R18	RES1	5A6
R19	RES1	5A6
R21	RES1	7A8
R22	RES1	5A7
R23	RES1	5A7
R24	RES1	5B8
R25	RES1	5D7
R26	RES1	5D8
R27	RES1	5D8
R28	RES1	5A7
R29	RES1	5A6
R30	RES	5A3
R31	RES	5A3
R32	RES1	5A6
R33	RES1	8A1
R34	RES1	8A1
R35	RES	5A3
R36	RES	5A3
R37	RES1	5A6
R38	RES	5A7
R39	RES	5A3
R40	RES	5A4
R41	RES	5A3
R42	RES	5A4
R43	RES	5A3
R44	RES1	5A7
R45	RES	5A3
R46	RES1	5B7
R47	RES1	5A7
R48	RES1	5A6
R49	RES1	5A7
R50	RES	5A3
R51	RES	5B4
R52	RES	5B4
R53	RES	5A3
R54	RES1	3B6
R55	RES1	3B6
R56	RES	3B5
R57	RES	3B6
R58	RES	3D7
R59	RES	3C7
R60	RES	3A5
R61	RES1	5A7
RJ1	RJ48_CON	3C3
SW1	SWITCH_DPDT_SLIDE_6P	3A6
T1	XFMR_2IN_4OUT_U	3B5 3D5
TP1	TSTPNT_SNG	7B2
TP2	TSTPNT_SNG	7B2
TP3	TSTPNT_SNG	7B2
TP4	TSTPNT_SNG	7C2
TP5	TSTPNT_SNG	7C2
TP6	TSTPNT_SNG	7B2
TP7	TSTPNT_SNG	7B2
TP8	TSTPNT_SNG	7B2
TP9	TSTPNT_SNG	7B2
TP10	TSTPNT_SNG	7B2
TP11	TSTPNT_SNG	7B2
TP12	TSTPNT_SNG	5D2
TP13	TSTPNT_SNG	5D2
TP14	TSTPNT_SNG	5A6
TP15	TSTPNT_SNG	5A6
TP16	TSTPNT_SNG	7B2
TP17	TSTPNT_SNG	5D2
TP18	TSTPNT_SNG	5A6
TP20	TSTPNT_SNG	7B2
TP21	TSTPNT_SNG	7B1
TP22	TSTPNT_SNG	7B1
TP23	TSTPNT_SNG	10A7
TP24	TSTPNT_SNG	10A8
TP25	TSTPNT_SNG	10A7
TP26	TSTPNT_SNG	10A7
TP27	TSTPNT_SNG	10A7
TP28	TSTPNT_SNG	10A7
TP29	TSTPNT_SNG	10A7
TP30	TSTPNT_SNG	10A7
TP31	TSTPNT_SNG	10A4
TP32	TSTPNT_SNG	10A4
TP33	TSTPNT_SNG	10A5
TP34	TSTPNT_SNG	10A5
TP35	TSTPNT_SNG	10A5
TP36	TSTPNT_SNG	10A5
TP37	TSTPNT_SNG	10A5
TP38	TSTPNT_SNG	10A5
U1	IDTQS3R861_U	6B3
U2	IDTQS3R861_U	6D3
U3	IDTQS3R861_U	6B6
U4	IDTQS3R861_U	6D6
U5	XILINX_XC9572XL	5D4 5D7
U6	IDTQS3R861_U	9B5
U7	IDTQS3125_U	9D3
U8	IDTQS3125_U	9D7
U9	IDTQS3125_U	9B3
U10	IDTQS3125_U	9B7
U11	DS2156_TQFP	2D7
Z1	SIDACTOR_2	3C4
Z2	SIDACTOR_2	3D5
Z3	SIDACTOR_2	3A5
Z4	SIDACTOR_2	3B5
Z5	SIDACTOR_2	3C6
Z6	SIDACTOR_2	3A4
Z7	SIDACTOR_2	3C4
Z8	SIDACTOR_2	3A4
Z9	SIDACTOR_2	3C4
Z10	SIDACTOR_2	3B4

TITLE: DS2156DK02

ENGINEER: SWS